Xavier Routh

xrouth2@illinois.edu | github.com/xavierrouth | https://xavierrouth.com

Education

University Of Illinois, Urbana-Champaign *Expected* **December 2024**
B.S Computer Engineering - 3.87 GPA (Dean's List 3 Semesters) Urbana-Champaign, IL
James Scholar Honors Program, HKN ECE Honors Society

Relevant Courses: Data Structures, Analog Signal Processing, Algorithms and Models of Computation, Digital Systems Laboratory (FPGAs), Applied Parallel Programming (CUDA)
Current: Compiler Construction, Computer Systems Engineering, Cryptography, Programming Languages

Experience

LLVM Group, under **Professor Vikram Adve**, **May 2023 - Present**
Undergraduate Researcher Urbana-Champaign, IL

- Ported several hyperdimensional computing (HDC) applications from GPU or FPGA implementations to a custom language, Hetero-C++, to be used as benchmarks for the HPVM project.
- Wrote a C++ runtime library to support HDC operations for CPU targets within the HPVM framework.
- Helped develop LLVM passes to lower HDC intrinsics within LLVM IR. IR generated included custom memory management and tiling to reduce compile times and allow for future optimizations.

NASA Glenn Research Center **June - August 2022**
SCaN - Software Engineering Intern Cleveland, OH

- Developed software to monitor and control operation of the S-Band Ground Station at NASA GRC.
- Communicated with various hardware devices via serial commands, SCPI, and DLL interfaces.
- Used Python and PyQt5 to develop GUIs that allowed monitoring of signal power levels and weather conditions.
- Set up TCP socket connection to communicate sensor information remotely across computers.

Technical Projects

LC-3 Compiler

- Wrote a non optimizing compiler for a subset of C that targets LC-3 assembly. Implemented in C, then Rust.
- Includes custom memory management to avoid usage of dynamic memory and improve efficiency.
- Integrated compiler with Compiler Explorer to allow access to students using LC-3 in their coursework.
- Supported by ECE 220 course staff and provided as an official course resource.

NES Hardware Emulator

- Designed a semi cycle-accurate NES running on a FPGA board using SystemVerilog.
- Used Intel's Platform Designer to configure a NIOS II based SoC design to handle USB input and load system memory with game roms.
- Required re-designing various asynchronous components of the original system to work on an FPGA.
- Added support for certain channels of the NES's audio output.
- Able to play Donkey Kong, Super Mario Bros and more.

FPGA SLC-3 Processor

- Implemented a simplified version of the LC-3 architecture onto an FPGA using SystemVerilog and ModelSim.
- Allows for input from on-board switches and buttons at program runtime via memory-mapped IO.

CUDA Convolutional Neural Network

- Implemented the forward propagation stage of the LeNet-5 CNN architecture using CUDA and Nsight Compute.
- Used optimization techniques including tiling, kernel fusion, and streaming to improve memory bandwidth.
- Placed in the top 15 of final competition submissions, out of around 200 students.

Skills

Languages: C, C++, x86, CUDA, SystemVerilog, LLVM, Rust, Ocaml

Workflow: Git, Quartus Prime, WSL 2, Docker, CMake, Make, Bash, Linux

Involvement

ACM Sigarch and Sigplan
HKN Review Sessions, Tutoring, and Office Hours.

Interests

Computer Architecture, Game Engines, Embedded Systems, Compilers, Data-Oriented Design, FPGAs